REMARKS

Claims 1, 4-14, 17-27, and 29-30 are pending in the present application. Claims 1, 4-14, 17-26, and 30 have been allowed. Claim 28 was cancelled; claim 29 was amended. Reconsideration of the claims is respectfully requested.

Amendments were made to the specification to correct errors and clarify the specification. No new matter has been added by any of the amendments to the specification.

I. Objection to the Specification

The specification was objected to as being informal. With respect to definitions in the specification for V_T and V_{BE}, the Office Action states:

> Firstly, Applicant has pointed out where in the specification the terms, such as V_T and V_{BE} are defined in the specification. However, it would seem proper for clear understanding the equation that definitions for the terms therein be provided directly following the equation.

Paper No. 16, page 2. Applicant respectfully notes that the terms are defined immediately following the equation. Immediately following the equation, the specification reads:

> . . . V_T is the absolute value of threshold voltage, and V_{BE} is the base emitter voltage.

Specification, page 7, lines 5-7. Since the discussion of the equation is general at this point in the specification, with reference only to a block diagram (Figure 1) rather than a detailed circuit diagram (Figure 2), it is appropriate that the definitions not be linked to specific circuit elements at this point. Additionally, the specification has been amended in the description relating to Figure 2 to clarify how the terms relate to specific circuit elements depicted.

Therefore, the objection to the specification has been overcome.

II. 35 U.S.C. § 112, Second Paragraph (Definiteness)

Claims 27-29 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. This rejection is respectfully traversed.

The specification has been amended as described above.

Additionally, Applicant respectfully notes that no equation appears in claim 27, and specifically the terms objected to are not found in claim 27. The reasons for the rejection stated in the Office Action bridging pages 2-3 are therefore seen as being directed to claim 28. Applicant has canceled claim 28, which is seen as essentially duplicating independent claim 1, as amended.

Therefore, the rejection of claims 27-29 and the objection to the specification under 35 U.S.C. § 112, second paragraph has been overcome.

III. 35 U.S.C. § 102 (Anticipation)

Claims 27-28 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Bingham*. This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Claim 27 reads:

> 27. (amended) A direct current sum bandgap voltage comparator comprising:
>
> a power supply having a predetermined threshold voltage level which defines the minimum acceptable voltage level of the power supply;
>
> a summing node;
>
> a plurality of current sources connected to the summing node and directly connected to a power supply voltage, each current source further comprising at least one transistor, and each current source supplying a current to the summing node; and
>
> an indicator circuit having an input connected to a summing node, wherein the indicator circuit is responsive to changes in the summing node voltage level and generates at an output a logical signal at one state when the summing node voltage is greater than the predetermined threshold voltage level and

> generates the logical signal at the output at another state when the summing node voltage level is less than the predetermined threshold voltage level.

Bingham does not disclose the claimed invention. Neither power supply disclosed in *Bingham*--that is, neither primary power supply connected to input 24 nor auxiliary power supply connected to input 26--has "a predetermined threshold voltage level which defines the minimum acceptable voltage level of the power supply." Instead, the power supplies provide whatever power they can and the switching circuit 10 switched between them depending on which power supply has the highest voltage level. *Bingham*, Figure 1; column 2, line 64 - column 3 line 38.

Comparator 36 in Figure 3 is a simple differential comparator, not a direct current sum bandgap voltage comparator. *Bingham*, Figure 2; column 4, line 38. Device 56 in Figure 3 is a simple inverter, not a comparator. *Bingham*, Figure 2; column 5, lines 21-22.

The output node 52 is not a summing node, but is a simple comparator output indicating which comparator input is higher for the purpose of switching between different power supplies:

> If the electrical potential appearing at the first input **24** is greater than the potential appearing at the second input **26**, the output **52** of the differential comparator **36**, coupled to the control input **54** of transistor **40**, turns on transistor **40**, thereby allowing transistor **40** to conduct power from the primary power supply at the first input to the output **30**.
>
> The output **52** of the differential comparator **36** is also coupled to an inverter **56**. If the second input **26** has a greater potential than the first input **24**, the output **52** of the differential comparator **36** turns off the transistor **40**. In addition, the output **52** of the comparator **36**, is inverted by the inverter **56**. The output **58** of the inverter **56**, coupled to the control input **60** of transistor **48**, turns on the transistor **48**, thereby enabling conduction of the auxiliary or backup battery power appearing at the second input **26** to the output **30**.

Bingham, column 3, line 54 - column 4, line 2.

Transistors 110 and 116 do not comprise current sources; rather, transistors 98 and 104 comprise a first current source while transistors 92 and 116 comprise a second current source. The first current source--transistors 98 and 104--is neither

connected to node 52 (the purported "summing node") nor directly connected to a power supply voltage. Instead, the output 106 of the current mirror is connected to the gate of transistor 110. while the current mirror is connected to transistor 40 and/or diode 62 which is connected in turn to power supply input 24. Thus, "a plurality of current sources connected to the summing node and directly connected to a power supply voltage" is not disclosed.

Therefore, the rejection of claims 27-28 under 35 U.S.C. § 102 has been overcome.

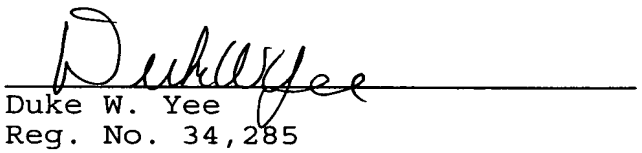
IV. Conclusion

It is respectfully urged that the subject application is patentable over *Bingham* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: March 13, 1997

Respectfully submitted,



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